ABSTRACT

Method for encoding and decoding composite VLIW packets and for performing related simulations has been disclosed. To accomplish the encoding of a composite VLIW packet, a bit pattern for a template in the VLIW packet must be determined and placed in the VLIW packet along with the bit patterns corresponding to each individual instruction in the VLIW packet. To accomplish the decoding of a composite VLIW packet, assembly code is provided for the bit patterns corresponding to each individual instruction in the VLIW packet. The bit pattern for the template in the VLIW packet is then matched against a known template. The known template uniquely corresponds to a known syntax. The known syntax is then matched to a resolved packet syntax. The resolved packet syntax is then used to provide assembly code associated with the execution of the combination of instructions in the VLIW packet. To accomplish the simulation of a composite VLIW packet, fetching a composite VLIW packet is simulated. The VLIW packet is then decoded, as above, to provide assembly code associated with the execution of the combination of instructions in the VLIW packet. Issuing of individual instructions is then simulated, for example, by placing the individual instructions in an instruction window. Allocation of execution units can then be simulated, for example, by the allocation of execution units to the individual instructions according to the instruction slot assignments in the VLIW packet. Execution of each individual instruction by its allocated execution unit is then simulated.